## Amendments to the Claims

Claims 1 to 12. (Cancelled)

13. (Currently Amended) A switch for switching time division multiplexed (TDM) data and packet data from input ports to output ports, comprising:

(A) means for switching a TDM data from an input port to an output port, comprising:

~~means for receiving a TDM data at the input port;~~

~~means for determining the output port to route the TDM data;~~

means for storing the TDM data in ~~selecting an address of~~ a single shared memory ~~for the TDM data~~ based on a time slot of a frame in which the TDM data was received;

~~means for storing the TDM data at the address in said shared memory;~~

~~means for reading the TDM data from the address in said shared memory;~~ and

~~means for transmitting the TDM data from the output port;~~ and

(B) means for switching a packet data from an input port to an output port, comprising:

~~means for receiving a packet data at the input port;~~

~~means for determining the output port to route the packet data;~~

means for storing the packet data in ~~selecting an address of~~ said single shared memory ~~for the packet data~~ based on routing data embedded in the packet data and based on the input port which received the packet data;

~~means for storing the packet data at the address in said shared memory;~~

~~means for reading the packet data from the address in said shared memory; and~~

~~means for transmitting the packet data from the output port;~~

~~wherein switching packet data has neither latency nor jitter effect on switching TDM data.~~

Claims 14 to 20. (Cancelled)

21. (Currently Amended) A switch to switch time division multiplexed (TDM) data and packet data from input ports to output ports, comprising:

a plurality of input ports to receive data, wherein each data comprises either TDM data or packet data;

a plurality of output ports to transmit switched data;

a single shared memory coupling said input ports to said output ports, said single shared memory to receive sequentially all TDM data and all packet data received from said input ports, said single shared memory to store both TDM data and packet data, said single shared memory to switch all sequentially received TDM data and packet data received from respective input ports to respective output ports, ~~wherein switching of any received packet data by said single shared memory has neither latency nor jitter effect on switching of any received TDM data by said single shared memory,~~ and wherein switching of any received TDM data is based on input time slots of said TDM data;

a time slot interchange controller coupled to said single shared memory to select addresses in said single shared memory to store TDM data, said time slot interchange controller to select an address of said single shared memory for a TDM data based on a time slot of a frame in which said switch received the TDM data; and

a packet ~~packed~~ switch controller coupled to said single shared memory to select addresses in said single shared memory to store packet data, said packet switch controller to select an address of said single shared memory for a packet data based on routing data embedded in the packet ~~packed~~ data and based on the input port which received the packet data.

22. (Previously Presented) A switch as claimed in claim 21, wherein each data is received by an input port as a time slot in a frame.

23. (Previously Presented) A switch as claimed in claim 21, wherein said single shared memory comprises a TDM data memory portion and a packet data memory portion.

24. (Previously Presented) A switch as claimed in claim 21, wherein said single shared memory treats the input ports as logical input ports.

25. (Previously Presented) A switch as claimed in claim 21, wherein said single shared memory to place sequentially received packet data in a queue for a respective output port.

26. (Previously Presented) A switch as claimed in claim 21, wherein the data are received by said input ports and transmitted by said output ports as data exchange units.

27. (Cancelled)

28. (Previously Presented) A switch as claimed in claim 21, wherein the switching of a data from a respective input port to a respective output port is controlled by a stored switch configuration.

29. (Previously Presented) A switch as claimed in claim 21, further comprising:

an input data router to route sequentially data from said input ports to said single shared memory; and

an output data router to route sequentially data from said single shared memory to said output ports.

30. (Previously Presented) A switch as claimed in claim 21, wherein the data are received by said input ports and transmitted by said output ports as data exchange units, the data exchange units for packet data comprise routing information, the switching of a data exchange unit from a respective input port to a respective output port is controlled by a stored switch configuration, said stored switch configuration uses the routing information of data exchange units for packet data to determine respective output ports to switch the data exchange units.

31. (Currently Amended) A method for switching time division multiplexed (TDM) data and packet data from input ports to output ports, comprising the steps of:

(A) switching a TDM data from an input port to an output port, comprising the steps of:

~~receiving a TDM data at the input port;~~

~~determining the output port for the TDM data;~~

storing the TDM data in ~~selecting an address of~~ a single shared memory ~~for the TDM data~~ based on a time slot of a frame in which the TDM data was received;

~~storing the TDM data at the address in said shared memory;~~

~~reading the TDM data from the address in said shared memory; and~~

~~transmitting the TDM data from the output port;~~ and

(B) switching a packet data from an input port to an output port, comprising the steps of:

~~receiving a packet data at the input port;~~

~~determining the output port for the packet data;~~

~~selecting an address of said single shared memory for the packet data;~~

storing the packet data ~~at the address~~ in said shared memory;

~~reading the packet data from the address in said shared memory; and~~

~~transmitting the packet data from the output port;~~

~~wherein switching the packet data has neither latency nor jitter effect on switching the TDM data~~.

32. (Previously Presented) The method of claim 31, wherein the preselected area of said single shared memory for storing the TDM data is based on a time slot in a frame in which the TDM data was received by the input port.

33. (Previously Presented) The method of claim 31, wherein the output port for the TDM data is determined based on a time slot in a frame in which the TDM data was received by the input port, and wherein the output port for the packet data is determined based on routing data embedded in the packet data and based on the input port which received the packet data.

34. (Currently Amended) A switch for switching time division multiplexed (TDM) data and packet data from input ports to output ports, comprising:

(A) means for switching a TDM data from an input port to an output port, comprising:

~~means for receiving a TDM data at the input port;~~

~~means for determining the output port for the TDM data;~~

means for storing the TDM data in ~~selecting an address of~~ a single shared memory ~~for the TDM data~~ based on a time slot of a frame in which the TDM data was received;

~~means for storing the TDM data at the address in said shared memory;~~

~~means for reading the TDM data from the address in said shared memory; and~~

~~means for transmitting the TDM data from the output port;~~ and

(B) means for switching a packet data from an input port to an output port, comprising:

~~means for receiving a packet data at the input port;~~

~~means for determining the output port for the packet data;~~

~~means for selecting an address of said single shared memory for the packet data;~~

means for storing the packet data ~~at the address~~ in said shared memory;

~~means for reading the packet data from the address in said shared memory; and~~

~~means for transmitting the packet data from the output port;~~

~~wherein switching the packet data has neither latency nor jitter effect on switching the TDM data~~.

35. (Currently Amended) A switch for switching time division multiplexed (TDM) data and packet data from input ports to output ports, comprising;

a plurality of input ports to receive data, wherein each data comprises either TDM data or packet data;

a plurality of output ports to transmit switched data;

a shared memory coupling said input ports to said output ports, said shared memory to receive sequentially the data received from said input ports, said shared memory to switch a sequentially received data from a respective input port to a respective output port~~, wherein switching of packet data by said shared memory has no latency or jitter effect on switching of TDM data by said shared memory~~;

a timeslot interchange controller coupled to said shared memory to select addresses in said shared memory to store TDM data, said time slot interchange controller to select an address of said shared memory for a TDM data based on a time slot of a frame in which said switch received the TDM data; and

a packet switch controller coupled to said shared memory to select addresses in said shared memory to store packet data, said packet switch controller to select an address of shared memory for a packet data based on routing data embedded in the packet data and based on the input port which received the packet data.

36. (Previously Presented) A switch as claimed in claim 35, wherein each data is received by an input port as a time slot in a frame.

37. (Previously Presented) A switch as claimed in claim 35, wherein said shared memory comprises a TDM data memory portion and a packet data memory portion.

38. (Previously Presented) A switch as claimed in claim 35, wherein said shared memory treats the input ports as logical input ports.

39. (Previously Presented) A switch as claimed in claim 35, wherein said shared memory places sequentially received packet data in a queue for a respective output port.

40. (Previously Presented) A switch as claimed in claim 35, wherein the data are received by said input ports and transmitted by said output ports as data exchange units.

41. (New) A switch to switch time division multiplexed (TDM) data and packet data from input ports to output ports, comprising:

a plurality of input ports to receive TDM data and packet data, each TDM data having an associated time slot of a frame;

a plurality of output ports to transmit switched data;

a single shared memory to switch TDM data and packet data from said input ports to said output ports, said single shared memory to store TDM data received at said input ports based on said time slot of said frame of each TDM data, said single shared memory to store packet data received at said input ports based on routing data embedded in each packet data and based on which input port received each packet data.

42. (New) A switch as claimed in claim 41, wherein said single shared memory comprises a TDM data memory portion and a packet data memory portion.

43. (New) A switch as claimed in claim 41, wherein said single shared memory to treat the input ports as logical input ports.

44. (New) A switch as claimed in claim 41, wherein said single shared memory to place sequentially received packet data in a queue for a respective output port.

E4 Cont

45. (New) A switch as claimed in claim 41, wherein said input ports to receive and said output ports to transmit TDM data and packet data as data exchange units.

46. (New) A switch as claimed in claim 45, wherein the data exchange units for packet data comprise routing information used to determine output ports to switch the data exchange units.

47. (New) A switch as claimed in claim 41, further comprising:

an input data router to route TDM data and packet data sequentially from said input ports to said single shared memory; and

an output data router to route TDM data and packet data sequentially from said single shared memory to said output ports.

48. (New) A switch as claimed in claim 41, further comprising:

a time slot interchange controller external to and coupled to said single shared memory to direct said single shared memory regarding storage of TDM data; and

a packet switch controller external to and coupled to said single shared memory to direct said single shared memory regarding storage of packet data.

49. (New) A system to switch time division multiplexed (TDM) data and packet data from input ports to output ports, comprising:

said switch of claim 41; and

a stored switch configuration coupled to said switch to control switching of said TDM data and packet data from said input ports to said output ports.

Ct Cont

50. (New) A method to switch time division multiplexed (TDM) data and packet data, comprising:

receiving TDM data and packet data at a plurality of input ports;

storing received TDM data in a single shared memory based on a time slot of a frame of each TDM data;

storing received packet data in said single shared memory based on routing data embedded in each packet data and based on which input port received each packet data; and

forwarding stored TDM data and packet data from said single shared memory to said output ports.

51. (New) The method of claim 50, wherein TDM data are stored in a preselected area of said single shared memory based on said time slots of said frames.

52. (New) The method of claim 51, wherein packet data are stored in an area other than said preselected area of said single shared memory.

53. (New) The method of claim 50, wherein the output ports for TDM data are determined based on said time slot of said frames, and wherein the output ports for packet data are determined based on said embedded routing data and based the input ports which received the packet data.